AMENDMENTS

In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A phase frequency detector comprising:

a phase error detector outputting a phase error signal according to a first input signal and a second input signal;

a phase error judgment unit outputting a phase error judgment signal according to the first input signal and the second input signal; and

a reset unit outputting a first reset signal according to the phase error judgment signal and receiving a clock signal, the first reset signal resetting the phase error detector, wherein the outputting of the first reset signal is triggered by the clock signal.

2. (Original) The phase frequency detector according to claim 1, wherein the phase error judgment unit is reset according to the first reset signal.

3. (Original) The phase frequency detector according to claim 1, wherein the reset unit further outputs a second reset signal according to the phase error judgment signal, the second reset signal resetting the phase error judgment unit.

4. (Original) The phase frequency detector according to claim 1, wherein whenever there exists a substantial phase error between the first and second input signals, the phase error signal remains active for such a certain period of time that a post-stage circuit senses the existence of the phase error.

5. (Original) The phase frequency detector according to claim 1, wherein the phase error judgment signal is active when transitions are detected in both the first input signal and the second input signal.

6. (Original) The phase frequency detector according to claim 1, wherein the phase error detector comprises:

a first flip-flop receiving the first input signal; and

a second flip-flop receiving the second input signal;

wherein an output of the first flip-flop resets the second flip-flop, and independently an output of the second flip-flop resets the first flip-flop.

7. (Original) The phase frequency detector according to claim 1, wherein the phase error judgment unit comprises:

a third flip-flop receiving the first input signal;

a fourth flip-flop receiving the second input signal; and

a phase error judgment signal output unit coupled to the third and fourth flip-flops for outputting the phase error judgment signal.

8. (Original) The phase frequency detector according to claim 1, wherein the reset unit comprises a reset flip-flop receiving the phase error judgment signal, for generating the first reset signal.

9. (Original) The phase frequency detector according to claim 1, wherein the reset unit comprises:

a fifth flip-flop receiving the phase error judgment signal; and

a sixth flip-flop receiving the phase error judgment signal.

10. (Original) The phase frequency detector according to claim 7, wherein the reset unit further comprises:

a seventh flip-flop coupled to the fifth flip-flop; and

an eighth flip-flop coupled to the sixth flip-flop.

11. (Currently Amended) A phase locked loop, comprising:

a phase frequency detector outputting a phase error signal according to a first input signal and a second input signal;

a quantizer outputting a count signal according to the phase error signal; and

an oscillator generating the second input signal according to the count signal;

wherein the phase frequency detector comprises:

a phase error detector outputting the phase error signal according to the first input signal and the second input signal;

a phase error judgment unit outputting a phase error judgment signal according to the first input signal and the second input signal; and

a reset unit outputting a first reset signal according to the phase error judgment signal, ~~to~~ the first reset signal resetting the phase error detector, wherein the quantizer is triggered by a clock signal, and the reset unit is also triggered by the clock signal.

12. (Original) The phase locked loop according to claim 11, wherein the phase error judgment unit is reset according to the first reset signal.

13. (Original) The phase locked loop according to claim 11, wherein the reset unit further outputs a second reset signal according to the phase error judgment signal, the second reset signal resetting the phase error judgment unit.

14. (Original) The phase locked loop according to claim 11, wherein whenever there exists a substantial phase error between the first and second input signals, the phase error signal remains active for such a certain period of time that the quantizer outputs a count value in the count signal.

15. (Original) The phase locked loop according to claim 11, wherein the phase error judgment signal is active when transitions are detected in both the first input signal and the second input signal.

16. (Canceled)

17. (Original) The phase locked loop according to claim 11, wherein the phase error detector comprises:

a first flip-flop receiving the first input signal; and

a second flip-flop receiving the second input signal;

wherein an output of the first flip-flop resets the second flip-flop, and independently an output of the second flip-flop resets the first flip-flop.

18. (New) A phase frequency detector comprising:

a phase error detector outputting a phase error signal according to a first input signal and a second input signal;

a phase error judgment unit outputting a phase error judgment signal according to the first input signal and the second input signal; and

a reset unit outputting a first reset signal and a second reset signal according to the phase error judgment signal, the first reset signal resetting the phase error detector, the second reset signal resetting the phase error judgment unit.

19. (New) A phase frequency detector comprising:

a phase error detector outputting a phase error signal according to a first input signal and a second input signal;

a phase error judgment unit outputting a phase error judgment signal according to the first input signal and the second input signal; and

a reset unit outputting a first reset signal according to the phase error judgment signal, the first reset signal resetting the phase error detector;

wherein the phase error judgment unit comprises a third flip-flop receiving the first input signal, and a fourth flip-flop receiving the second input signal.